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NEW CONCEPTS FOR SOLID STATE MICROWAVE GENERATORS

Report No. 1

Contract No. DA 36-039 AMC 00001 (E)

Project No. DA 3A99-001

Period Covered

First Quarterly Report

1 October 1962 to 31 December 1962

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U. S. Army Electronics Agency

Fort Monmouth, New Jersey

Shockley Laboratory
Clevite Transistor Division
Clevite Corporation
Palo Alto, California

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Report Prepared By

R. M. Scarlett

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1. PURPOSE

The purpose of this contract is to extend the application of solid-state devices in the microwave region. To this end, specific devices, in particular the transit-time delay diode, are to be explored for their theoretical potential and practical capability.

2. ABSTRACT

The basic theory of transit-time delay diodes is presented, and their maximum power output calculated. This output is about 13% of that calculated for conventional transistors on a similar basis, but the maximum operating frequency should be much higher. It is shown how the maximum voltage decreases with frequency, leading to a lower impedance level. Experimental devices designed to make use of delay in the collector depletion layer did not show negative resistance because of difficulty in operating at the required voltage.

The reverse recovery of a PIN diode is calculated and shown to be useful for harmonic generator applications. The transition time from on to off is determined by the transit time for carriers across the I region in space-charge limited flow, and by the diode capacitance. Experimental epitaxial diodes showed the expected performance of less than 1 ns turn-off time in a diode with 15 pf capacitance.

3. PUBLICATIONS

Monthly performance summaries have been delivered to the contracting officer as required. On 24 October 1962, Dr. Kurt Hubner visited Dr. Ernest Schiel at Fort Monmouth to discuss work planned for this contract.

4. FACTUAL DATA

4.1 Introduction

The present contract calls for the exploration of new means of generating microwave power with solid-state devices. During the first quarter, work was directed toward two devices which appeared to show promise for applications in the low microwave region. These devices are the transit-time delay diode for direct generation of rf power from a dc source, and the PIN charge-storage diode for harmonic generation from an rf source of lower frequency. Sections 4.2 and 4.3 below describe the basic theory of these devices, construction of experimental models, and measured performance.

4.2 Transit-time Delay Diodes

The transit-time delay diode was first described by Shockley,[1] who presented the fundamental theory and derived certain limits on the negative resistance obtainable with practical devices. A later paper by Gibbons[2] reviewed this theory and pointed out its relation to conventional modes of transistor operation. More recently, results obtained by Zuleeg and Vodicka[3] on the microwave operation of drift transistors led them to conclude that the transit-time mode of operation was responsible for producing power at frequencies greater than the conventional cut-off frequency of the transistors. However, there appears to have been little work reported in the literature on the optimum design of devices for this purpose and practical limits of performance.

4.2.1 Basic Theory

The transit-time delay diode is essentially a transistor in which use is made of the delay of minority carriers in crossing the base region

to produce a two-terminal impedance with a negative real part in certain frequency bands. The operation depends on the fact that the average carrier delay time can be greater than one-half of the rf period, so that transit angles of greater than 180° occur. Unfortunately, dispersion of the delay time caused by diffusion results in the rf signal being attenuated to an unuseable degree unless the carriers move across the base principally by a built-in drift field.

Figure 1 is a schematic representation of the simplest form of device structure. The currents and voltages indicated are small-signal ac quantities superimposed on dc biases applied in the conventional manner for transistor operation. To show how negative resistance can arise, it is convenient to open-circuit the base terminal for ac so that $i_b = o$ and $i_c = i_e$, although other operating modes are possible. The ac voltage v_c from collector to emitter is assumed to appear entirely across the reverse-biased collector depletion layer. If the capacitance of this layer is C, a displacement current i_d flows, given by

$$i_d = j\ \omega\ C\ v_c \tag{1}$$

This displacement current establishes an ac current of holes (referring to an npn structure) into the base layer. To maintain space charge neutrality, an electron current must be injected at the emitter. The emitter efficiency is assumed to be unity, so that the emitter current $i_e = i_c$ consists entirely of minority carriers (electrons) injected into the base layer. These carriers diffuse and drift to the collector depletion layer, where they are swept into the collector. We shall denote by α the ratio of electron current arriving at the collector to that injected at the emitter. As indicated in Fig. 1, the total collector current is hence comprised of the displacement current i_d and the arriving minority current $\alpha\, i_c$:

$$i_c = i_d + \alpha\, i_c \tag{2}$$

By making use of Eq. (1), the impedance $Z_{ce} = v_c/i_c$ seen in the collector circuit at frequency ω is found to be:

$$\omega C Z_{ce} = j\alpha - j \qquad (3)$$

From this relation it is evident that at frequencies where α has a positive imaginary part, Z_{ce} will have a negative resistive component and ac power can be drawn from the device. This is the situation shown in the phasor diagram of Fig. 2. From similar triangles, it is seen that the component of v_c which is out of phase with i_c and represents ac power leaving the device, is proportional to α_i, the imaginary part of α.

The impedance Z_{ce} can be expected to vary with frequency in a manner like that shown in Fig. 3, which is a polar plot of α and of $j\alpha - j$ (see Eq. 3) with frequency as a parameter. A typical plot of α for a transistor with a built in drift field is sketched, starting at nearly $1 + j0$ for zero frequency, and progressing around the origin in a clockwise direction with increasing frequency. The imaginary part of α is positive for frequencies between f_1 and f_2, leading to a region where Z_{ce} has a negative resistance as shown in the dashed curve. This region occurs at frequencies higher by a factor of two or more than those used for conventional operation, which is generally limited to frequencies where the phase angle of α is of the order of -60° or less.[2]

It is advantageous to maximize the negative resistance obtained at a given frequency and capacitance. This is done by making the magnitude of α as large as possible and its phase angle around -270°. Evidently, the limiting case corresponds to the situation where the minority carriers move by drift only and experience delay without dispersion. In

that event, the magnitude of α is always unity and the maximum negative resistance is obtained for a transit angle of -270°, i.e. $\omega \tau_b = 3\pi/2$ where τ_b is the transit time delay across the base layer.

A strong built-in field to maximize drift with respect to diffusion is produced by a concentration gradient of impurity atoms in the base layer as indicated in the sketch of Fig. 4. The potential drop across the layer is given by $\Delta V = (kT/q) \ln N_1/N_c$, and the field is $E_b = \Delta V/w_b$. The drift time through the base is therefore

$$\tau_b = w_b/\mu E_b = w_b^2/\mu \Delta V = w_b^2/D \ln (N_1/N_c) \qquad (4)$$

where D is the diffusion constant for minority carriers. By comparison, the average time it takes for carriers to cross the base by diffusion is $\tau_{diff} = w_b^2/2D$. If $\ln (N_1/N_c)$ is large, the phase angle of the current gain α is controlled principally by the drift time of Eq. (4).

The current gain α for a number of different doping ratios N_1/N_c has been calculated by Shockley,[1] taking into account the effects of both drift and diffusion. The largest negative term in Z_{ce} occurs when the phase angle of α is around $-5\pi/4$. The normalized impedance $\omega C Z_{ce}$ of Eq. (3) is found to be as follows:

$$N_1/N_c = 10 \quad : \quad \omega C Z_{ce} = -0.05 - j\,1.065 \qquad (5a)$$

$$N_1/N_c = 10^2 \quad : \quad \omega C Z_{ce} = -0.116 - j\,1.14 \qquad (5b)$$

$$N_1/N_c = 10^3 \quad : \quad \omega C Z_{ce} = -0.156 - j\,1.18 \qquad (5c)$$

It is unlikely that larger values of N_1/N_c can be easily achieved in practical devices. This means that the negative resistance obtainable

is only a small fraction of the collector capacitive reactance $1/\omega C$, and attention must be paid to eliminating unnecessary ohmic resistance in the device.

4.2.2 Influence of the Depletion Layer

The transit time of minority carriers crossing the collector space-charge layer adds an additional phase angle to that produced by drift across the base layer, and could in principle be used to improve the magnitude of the negative resistance. The effect of the depletion layer can be expressed by the following transfer function $S(\omega)$ which is multiplied by α to obtain the overall current gain:

$$S(\omega) = \frac{\sin(\omega t_o/2)}{\omega t_o/2} \epsilon^{-\omega t_o/2} \qquad (6)$$

This function was derived on a previous Signal Corps contract,[4] and describes the ratio of ac current leaving the depletion layer to that entering. The time t_o is the transit time w_s/v_l across the layer, where v_l is the scattering-limited velocity which in N type Si is about 8×10^6 cm/sec for fields larger than 2×10^4 v/cm.[5] Equation (6) is conveniently characterized by a cutoff frequency ω_s

$$\omega_s \equiv 2/t_o = 2 v_l/w_s \qquad (7)$$

At ω_s, $S(\omega)$ has a -57° phase angle and an amplitude of 0.84. Above ω_s, the amplitude falls rapidly, so that this range is not useful. Equation (7) thus sets a limit to the maximum depletion layer width w_s for a given operating frequency ω as follows:

$$w_s < 2 v_l/\omega = 1.6 \times 10^7/\omega \qquad (8)$$

4.2.3 Collector Resistance Limitation

For a net negative resistance to be present, the ohmic resistance of the collector N^- layer (see Fig. 4) must be small. We shall estimate the minimum doping required, assuming that during part of the cycle the voltage is low and the entire thickness w_s of the N^- layer contributes to its resistance. It is further assumed that at maximum voltage V_B, the depletion layer just penetrates through w_s. These assumptions are reasonable if maximum power output is to be obtained. If the doping ratio N_1/N_c is 10^2, the maximum negative resistance from Eq. (5a) is nearly

$$-R = 0.12/\omega C \simeq 0.12\, w_s/2\, \epsilon\omega \text{ ohm-cm}^2 \tag{9}$$

where $2\epsilon/w_s$ has been used for the average capacity per unit area. The ohmic resistance of the N^- layer is

$$R_c = \rho_{(N^-)}\, w_s = w_s^2/\mu Q_B \text{ ohm-cm}^2 \tag{10}$$

where Q_B is the total charge of uncompensated donor atoms in the N^- layer, and is about 3×10^{-7} c/cm^2 for silicon under the above assumptions. If we require the ratio $R_c/-R$ to be less than 1/3, we obtain from (9) and (10) the following limits on $\rho_{(N^-)}$ and w_s:

$$\rho_{(N^-)} < 2 \times 10^{10}/\omega \text{ ohm-cm} \tag{11}$$

$$w_s < 6 \times 10^6/\omega \text{ cm} \tag{12}$$

where $\mu = 10^3$ cm^2/volt-sec and $\epsilon = 10^{-2}$ f/cm have been used as representative values for silicon. It is to be noted that the restriction on w_s of Eq. (12) will also satisfy the limit imposed by depletion layer transit time, as expressed in Eq. (8).

4.2.4 Maximum Power Output

We shall make a rough estimate of the power output per unit area on the basis of the maximum voltage and current which can reasonably be employed. The maximum peak voltage swing is

$$v_{cp} = V_B/2 = E_B w_s/4 \quad \text{volts} \tag{13}$$

where E_B is the breakdown field of about 3×10^5 V/cm, and w_s is the peak space-charge layer width (see Fig. 4). From the impedance expression of Eq. (5b), the peak out-of-phase current is then

$$i_{cp} \simeq 0.09\, v_{cp}\, \omega\, C = 0.045\, E_B\, \omega \epsilon \ \text{a/cm}^2 \tag{14}$$

using (13), since the average capacity is $2\epsilon/w_s$. The power output density is thus

$$P_{out} = \frac{i_{cp} v_{cp}}{2} = 0.18\, E_B^2\, \omega\, \epsilon\, w_s/16 \tag{15}$$

From Eqs. (7) and (12), the limitation on w_s because of series resistance considerations can be written as $w_s < 0.75\, v_f/\omega$, so that (15) becomes

$$P_{out\ max} = 0.13\, \epsilon\, E_B^2\, v_f/16 \ \text{watts/cm}^2 \tag{16}$$

This limit is 0.13 times the limit derived for the conventional mode of transistor operation in a previous Signal Corps contract.[6] However in the latter case, the limit is good only at frequencies of the order of the cut off frequency and below, while Eq. (16) applies to a frequency two to three times higher.

There are two additional factors which may modify Eq. (16). One of these is the influence of mobile charge in the space charge layer. This influence turns out to be small under the conditions used to derive Eq. (16). The other factor is the high injection limit, where the injected minority carriers begin to swamp out the built-in field in the base layer and degrade the negative impedance obtainable, and can be estimated as follows: The peak emitter current is about $i_e = v_{cp} \omega C = \epsilon E_B \omega/2$ from Eq. (14). Using relationships drived by Shockley,[1] one finds that the peak minority charge in the base layer is about $Q_m \simeq 2 i_e \tau_b/3 = \epsilon E_B \omega \tau_b/2 = 5\pi Q_B/8 \simeq 2 Q_B$, i.e. about twice the breakdown charge Q_B. To avoid influencing the built-in field, the total charge of impurity atoms in the base layer should be several times Q_m. This condition will be difficult to achieve for very thin layers corresponding to high frequencies; estimated values where the high-injection limit will be important are a base width of 1 μ corresponding to an operating frequency of around 3 Kmc for a silicon NPN device.

4.2.5 Experimental Devices

Two types of experimental npn devices of widely differing area were made by standard double diffusion techniques to obtain an impurity distribution qualitatively like that of Fig. 4. The expitaxial silicon starting material had a 5 ohm-cm N^- layer about 10 μ thick on a very low resistivity substrate. A base layer 2 μ thick with $N_1/N_C > 10^2$ was aimed at in order to achieve negative resistance around a frequency of 1.5 Kmc (see Eq. (4) with $\omega \tau_b = 10^{10} \tau_b = 5\pi/4$). This base layer was produced by a boron diffusion to a depth of about 2 μ and a surface concentration of 7×10^{19} cm^{-3}, followed by a phosphorus emitter diffusion 0.5 μ deep through an oxide mask. Aluminum contacts were evaporated and alloyed, the chip mounted on a TO-18 header, and gold leads attached by thermocompression bonding.

The small area device has a "horseshoe" geometry, with the emitter stripe surrounded on three sides by the base contact. Its emitter area is 6×10^{-5} cm^2, the collector junction area 3×10^{-4} cm^2, and the collector capacity at 10 volts is about 1.5 pf. The large area device has an interdigitated geometry with six emitter fingers, an emitter area of 3×10^{-3} cm^2, and a collector junction area of 6×10^{-3} cm^2 with a capacity at 10 volts of 30 pf.

Figure 5 shows normalized impedance measurements made on a General Radio Transfer Function and Immittance Bridge. The real and imaginary parts of the impedance were multiplied by ωC, and plotted with frequency in Mc as a parameter; shown are points for 160, 500, 920 and 1500 Mc. Unit 3-6 is a small area device, while unit 4-1 is of large area. The z parameters shown are those of the common emitter configuration; z_{22} (ac open base) is equivalent to Z_{ce} of Eq. (3), giving $\omega C z_{22} = j\alpha - j$, while z_{21} (v_c/i_b with ac open collector) is given by $-\alpha/j\omega C$ for the idealized situation of Fig. 1, so that $\omega C z_{21} = j\alpha$.

The general shapes of z_{22} and z_{21} for the small area device (3-6) conform to the expected shape given by the dotted curve in Fig. 3, except that the negative resistance region is not reached. The parasitic package impedances are larger than the rather low impedance of the large area device, making accurate measurement of the latter difficult at the higher frequencies.

The principal reason that negative resistance is not observed in Fig. 5 is probably the resistance R_c of the collector N^- layer. To compensate for this effect, each point on the curve of z_{22} should be shifted to the left by an amount $\omega C R_c$. For an estimated R_c of 15 Ω and $C = 1.5$ pf, this quantity is about 0.2 at 1500 Mc, sufficient to move the point into the negative resistance region. The collector

resistivity of 5 ohm-cm is excessive by the standards of Eq. (11), which specifies a maximum resistivity of 2 ohm-cm at 1500 Mc. It was hoped to operate the device at a sufficiently high voltage (100V) to sweep out most of the N^- layer and effectively remove its resistance, but power dissipation considerations did not permit this. Devices with lower (1 ohm-cm) collector resistivity are presently in process.

4.3 PIN Charge Storage Diodes

4.3.1 General

The second device on which work has been undertaken on this contract is a charge storage diode. Such devices are sometimes referred to as step recovery diodes or "snap-off" diodes. The ideal charge storage diode stores a large amount of charge at very low voltage in the forward direction, and very little charge at large reverse voltage. It thus acts like a nonlinear capacitor with an abrupt capacitance change around zero volts.

One useful application for charge storage diodes is that of harmonic generation. It appears that these diodes may have an advantage in efficiency over conventional varactor diodes for high-order harmonic generation in a single stage, where the complexity of intermediate idler circuits is undesirable.[7,8] Although the maximum theoretical performance of charge-storage has not been established, an analysis for the case of a resistive source and tuned load impedance has shown that the minimum loss in generating a harmonic of about tenth order or greater is around 8.5 db independent of the order of the harmonic.[9]

An ordinary PN junction provides an approximation to an ideal charge-storage diode, in that it exhibits a large capacitance in the forward direction (diffusion capacity) and a much smaller capacitance in the reverse direction (depletion-layer capacity). Unfortunately, the transition from forward to reverse does not take place in zero time, and a residual minority carrier charge is left in the diode if it is suddenly reversed biased following a period of forward bias. Means must be sought to minimize this residual charge without unduly increasing the reverse capacitance.

In general, the residual charge is minimized by insuring that the majority of the forward bias charge is stored close to the junction, so that it will have a short distance to diffuse when the junction is reverse biased. One approach to this situation has been to employ a steeply graded junction, whose retarding fields tend to confine minority carriers to the vicinity of the junction.[10] The steeper the gradient, the smaller will be the effect of residual charge, but the larger will be the reverse capacitance so that an optimum gradient exists for a given application.

It was suggested by Shockley[11] that a PIN diode might provide the best possible performance as a charge storage diode. With present epitaxial techniques, PIN or $P^+N^-N^+$ structures with appropriately thin and abrupt middle layers can be made much more readily than by diffusion. Accordingly, the next section presents an approximate theory for the dynamic behavior of a PIN diode, and the section following describes observations made on experimental devices.

4.3.2 PIN Diode Storage and Transition Times

A qualitative sketch of the transient carrier density and electric field distributions occuring when the current density is switched from a

value J_f in the forward direction to J_r in the reverse direction is shown in Fig. 6. An intrinsic region of width w exists between heavily doped P and N regions, so that the particle current is carried almost entirely by holes at the P-I junction and entirely by electrons at the I-N junction. The width w is assumed to be much less than a diffusion length; under this condition the forward current J_f establishes steady-state hole and electron densities $p_f = n_f$ which are nearly constant across the I layer:

$$Q_f = q\, n_f\, w = \tau\, J_f \tag{17}$$

where τ is the lifetime. When the current is reversed, it will be shown below that a rather low voltage (compared to the reverse breakdown voltage) remains across the diode until substantially all of the stored charge Q has been extracted or recombined. During the time, the charge Q of either carrier behaves according to

$$-J_r = Q/\tau + dQ/dt \tag{18}$$

If $Q = Q_f$ (Eq. 17) at the instant J_r is applied, one finds that $Q = 0$ after a time t_s given by

$$1 - \epsilon^{-t_s/\tau} = Q_f/J_r\tau = J_f/J_r \tag{19}$$

If J_f/J_r is small, the storage time t_s is approximately

$$t_s \simeq \tau\, J_f/J_r \tag{20}$$

It is sometimes convenient to apply a sinusoidal current $J_m \sin \omega t$ for purposes of measuring lifetime. If the recovery takes place less than abou 1/8 cycle after the current reverses (i.e. if $\omega t_s < \pi/4$), it is readily shown that the storage time t_s is nearly equal to τ.

We now consider carrier flow in the I region when the current is reversed. To simplify the discussion, we shall suppose that electrons and holes have equal mobility μ. This assumption does not alter the essential features of the recovery, and a more complete theory will be presented in a later report. We shall further suppose that the recovery takes place in a time short compared to the lifetime, so that recombination can be ignored.

Upon application of the current $-J_r$, the hole and electron distributions begin to move through each other. Electrons move out of the left side of the I layer (see Fig. 6) and holes out of the right side, leaving regions of width s (a function of time) in which carriers of only one sign are present. Current in these regions is thus carried by space-charge limited flow,[12] while the current in the center is carried by both holes and electrons until s becomes $w/2$ at time t_1. Prior to t_1, $n_f = p_f$ in the center remains constant, and for equal mobilities the field in the center is:

$$E_c = J_r / 2 q \mu n_f \tag{21}$$

where n_f is given by Eq. (17).

The following results are taken from the theory of space-charge limited flow.[12] The voltage across the region s is

$$V_s = (8 J_r / 9 \epsilon \mu) s^{3/2} \tag{22}$$

and the maximum field which occurs at the edges of the I region is

$$E_{s\,max} = (2 J_r / \epsilon \mu)^{1/2} s^{1/2} = 3 V_s / 2 s \tag{23}$$

where ϵ is the dielectric constant which is 10^{-12} f/cm^2 for silicon.

In deriving these relationships the effects of diffusion have been ignored because the voltages are generally large compared to kT/q so that the current is carried chiefly by drift. For these equations to be applicable, the minimum carrier density which occurs at the edges of the I region must be much less than n_f; This minimum density is

$$n_{min} = J_r/q\mu E_{s\,max} \tag{24}$$

An alternative formulation is that $E_{s\,max}$ must be much greater than E_c.

The transit time τ_s of a carrier through the s regions is found to be

$$\tau_s = (2\epsilon/\mu J_r)^{1/2} s^{1/2} = 2s/\mu E_{s\,max} \tag{25}$$

while the total charge of carriers Q_s in either s region is

$$Q_s = J_r \tau_s = \epsilon E_{s\,max} \tag{26}$$

Under conditions generally obtaining, the charge Q_s is calculated to be much less than the charge of $q n_f s$ which was in the s region prior to application of reverse current. This conclusion follows immediately from Eqs. (24) and (25) under the necessary assumption that $n_{min} << n_f$. As a result, for constant reverse current J_r, s increases linearly with time. The charge extracted from the diode at any instant is $Q = 2 q s n_f$, and since $dQ/dt = J_r$, s increases as

$$ds/dt = J_r/2 q n_f \tag{27}$$

When s reaches w/2 at $t = t_1$, the charge is almost all gone, and a new phase commences, as discussed below.

It has been implicitly assumed that all the current J_r is particle current, whereas in fact a portion of J_r will be displacement current. This portion is a maximum at the edges of the I region where E_s is increasing most rapidly, and is given by $\epsilon\, d\, E_{s\,max}/dt = d\,Q_s/dt$. The particle current, on the other hand, is dQ/dt where $Q = 2\,q\,s\,n_f$. As discussed above in connection with Eqs. (24), (25) and (26), Q_s is ordinarily much less than Q (except at the very beginning of the reverse transient), and thus displacement current can be ignored for $t < t_1$.

At $t = t_1$, the edges of the distributions cross each other. At this time, the voltage across the I layer is twice that given by Eq. (22), with $s = w/2$; this voltage is in general only a few volts, so the diode still appears to have low impedance. For $t > t_1$ a center region with no carriers in it develops, and the current in this region is carried entirely by displacement. The shape of the carrier distributions toward the edges and the field in the end regions remains static as the empty center region widens. When the field E_c in the center region has built up to $E_{s\,max}$, which is the field at the edges given by Eq. (23) with $s = w/2$, the carriers are all gone. The time at which this occurs is denoted by t_2. For $t > t_2$, the reverse current simply charges the capacitance $C = \epsilon/w$ across the I layer.

The time $t_2 = t_1$ is calculated by observing that during this time, the field in the center E_c is building up a rate of $dE_c/dt = J_r/\epsilon$. It starts from a relatively low value given by Eq. (21), and at t_2 reaches a much larger value $E_{s\,max}$ given by Eq. (23). The time interval $t_2 - t_1$ is thus $\epsilon\, E_{s\,max}/J_r$ which is

$$t_2 - t_1 = (w\,\epsilon/\mu J_r)^{1/2}$$

$$= \tau_s\,(s = w/2) \qquad (28)$$

It is noted that this transition time is just the transit time for a carrier in space-charge limited flow across the width w/2 (see Eq. (25)).

The voltage across the I layer at time t_1 is, from Eq. (23)

$$V_i(t_1) = 2 V_s = 2 E_{s\,max} w/3 \tag{29}$$

At time t_2, since the field is now $E_{s\,max}$ uniformly across the I layer, the voltage is

$$V_i(t_2) = E_{s\,max} w \tag{30}$$

an increase of only 1/3 from the value at t_1. For $t > t_2$, the voltage evidently increases as

$$dV_i/dt = J_r/C \tag{31}$$

$$C = \epsilon/w$$

For a numerical example, we choose conditions similar to those obtaining in the experimental diodes described in the next section. Consider the following values:

$$\begin{aligned} \epsilon &= 10^{-12}\ \text{f/cm} \\ \mu &= 500\ \text{cm}^2/\text{V-sec} \\ \tau &= 0.1\ \mu\text{sec} \\ w &= 5\ \mu = 5 \times 10^{-4}\ \text{cm} \\ J_f &= 10\ \text{a/cm}^2 \\ J_r &= 100\ \text{a/cm}^2 \end{aligned} \tag{32}$$

From the foregoing equations, one calculates the following quantities:

$$
\begin{aligned}
n_f &= 1.25 \times 10^{16}\ \text{cm}^{-3} \\
t_s \simeq t_1 &= 10\ \text{ns} \\
E_c,\ t < t_1 &= 50\ \text{V/cm} \\
E_{s\ max}\ \text{at}\ t_1 &= 10^4\ \text{V/cm} \\
V_i\ \text{at}\ t_1 &= 3.3\ \text{volts} \\
t_2 - t_1 &= 10^{-10}\ \text{sec} = 0.1\ \text{ns} \\
V_i\ \text{at}\ t_2 &= 5\ \text{volts} \\
dV_i/dt,\ t > t_2 &= 50\ \text{volts/ns}
\end{aligned}
\tag{33}
$$

Thus a storage time of 10 ns is expected. The voltage across the diode at the end of the storage phase is 3.3 volts, which is small compared to the expected reverse breakdown voltage of about 150 volts. The transition time $t_2 - t_1$ is very fast, and from then on the diode behaves like a small capacitor. It is evident that faster rates can be achieved with higher current densities.

4.3.3 Experimental PIN Diodes

To approximate a PIN diode, a P N^-N^+ structure was made by diffusing a heavily doped boron layer about 2 μ deep into expitaxial material having a 15 ohm-cm region 5 μ thick on a heavily doped substrate. Mesas of 0.8 mm and 1.2 mm diameter were etched, aluminum contacts evaporated, and the devices packaged in a small glass package about 1/4" long. At reasonable current densities (10 A/cm^2 or more), the hole and electron densities in the N^- region are much larger than the density of doping atoms, and the diode is then equivalent to a PIN.

It was found that the turn-off speed of the diode depends upon the abruptness of the transition from N^- to N^+ at the epitaxial interface. The distribution of doping in this region is studied by means of capacitance vs. reverse voltage measurements in the following way. For a certain voltage V, the space charge layer extends a distance w from the P^+N^- junction, and w is determined from $w = \epsilon/C$, where C is the capacitance per unit area. If the voltage is increased by dV, an additional charge $dQ = CdV = q\,N(w)\,dw$ is exposed, where N(w) is the doping density at w. But $dw = -(\epsilon/C^2)\,dC$. Thus

$$CdV = -q\,N\,\epsilon\,dC/C^2 \tag{34}$$

so that N can be determined from the capacity, and the rate of capacity change with voltage dC/dV. It is convenient to plot C vs. V on log-log paper, and to use the slope obtained from such a plot. Eq. (34) can be written

$$N = -(C^2\,V/q\epsilon)\,d\log V/d\log C \tag{35}$$

Figure 7 shows N vs. distance for 3 PIN diodes as obtained from capacitance measurements and Eq. (35). Diodes No. 5-6 and 2-5 are large and small area diodes respectively, and exhibit turn-off times which are limited by their capacities. Diode 2-9 has a much more gradual transition to the N^+ region, and its turn-off time is considerably slower. Part of this increase in turn-off time is caused by the wider "I" layer. In addition to this, it is believed that minority carriers stored in the transition region between N^- and N^+, where the approximation to intrinsic material no longer holds, are partly responsible for the increase.

The experimental diodes were examined for their reverse recovery behavior in the circuits of Fig. 8 and 9. In Fig. 8, a current sine wave of about 2 amperes peak is applied to the diode under test when the four-layer diode fires. The first half-cycle is in the forward direction, and lasts for about 250 ns. When the current reverses, the voltage across the diode remains low until nearly all the carriers have been extracted. According to the discussion in connection with Eq. (20), the time between current reversal and voltage recovery is approximately equal to the effective lifetime, if this occurs in less than 1/4 cycle.

In the circuit of Fig. 9, a steady forward current I_f flows through the 250 ohm resistor, and a pulsed reverse current is applied by means of the pulse generator V_p. The voltage across the diode is observed by means of a sampling-type oscilloscope with a rise time of 0.4 ns.

Waveforms of the diode voltage photographed in the circuit of Fig. 9 for various combinations of forward and reverse current are shown in Figs. 10 and 11. The overshoot and ringing following the sharp transition is due to inductance in the diode package. In Fig. 10, which is a small area diode, the transition takes place in about 1 ns. The capacitance of this diode is about 15 pf, and the load resistance in the circuit during the transition is 25 ohms, so one would expect a 10-90% rise time of $2.2\ RC \simeq 0.8$ ns. One can thus conclude that the observed transition time is largely caused by charging the diode reverse-bias capacitance. By virtue of Eq. (20), the lifetime of this diode is about 40 ns from the fact that the storage time for I_f = 500 mA, I_r = 1 amp is 20 ns in Fig. 10.

Figure 11 shows waveforms for a large area diode whose capacitance is about 40 pf. The transition time is larger than that of

Fig. 10 by nearly the ratio of the capacitances. The effective lifetime of this particular diode is about 80 ns. Variations of the order of two to one in lifetime were found among both small and large diodes.

Figure 12 illustrates waveforms obtained in the circuit of Fig. 8. Two small area diodes from the same batch are shown, one of which had been subjected to a gold diffusion at 950 °C. The effect of this gold treatment is to lower the lifetime from 80 ns to 30 ns. Such lifetime control may be of use in certain applications of charge storage diodes.

It is evident that the observed transition times are limited by the diode capacitances, and that smaller area diodes should exhibit appreciably lower transition times. It is planned to make some of these during the next quarter, and to compare their performance with that obtainable from other types of charge-storage diodes.

5. CONCLUSIONS

Transit-time devices can theoretically deliver a power per unit area which is about 13% of that obtainable from conventional transistors. The maximum frequency of operation of units with comparable dimensions should, however, be higher by a factor of the order of three. From the experimental results, it does not appear feasible to make substantial use of the delay occurring in the collector depletion layer, particularly if maximum power is to be obtained. The lower impedance level necessary at higher frequencies may cause practical difficulties in large area devices.

It appears that PIN diodes can provide excellent performance as charge-storage diodes. The limiting factor in all but very high voltage units is probably the reverse capacitance. Experimental diodes had

turn-off times controlled largely by their capacitance; it has not yet been determined how far this can be reduced before transit-time effects limit the speed.

6.. PROGRAM FOR NEXT QUARTER

Work will continue on both transit-time and PIN devices. The former will be made on lower resistivity collector material to avoid the limitation due to collector resistance. Oscillator circuits will be built to test the power output of experimental devices in the 1.5 Kmc region.

PIN diodes of smaller capacitance than those reported here will be made in an attempt to approach fundamental limits set by transit time. It is felt that this work may then form a fairly complete package, so that this effort may be diverted to further assist with the transit-time device. A decision will be made in consultation with the appropriate people at Fort Monmouth before the end of the next quarterly period.

7. PERSONNEL

The following personnel contributed to work on this contract during the first quarter:

Senior Scientists

R. M. Scarlett
K. Hubner

Associate Scientist

M. Yamada

Technicians

John Luetscher
William Margolis

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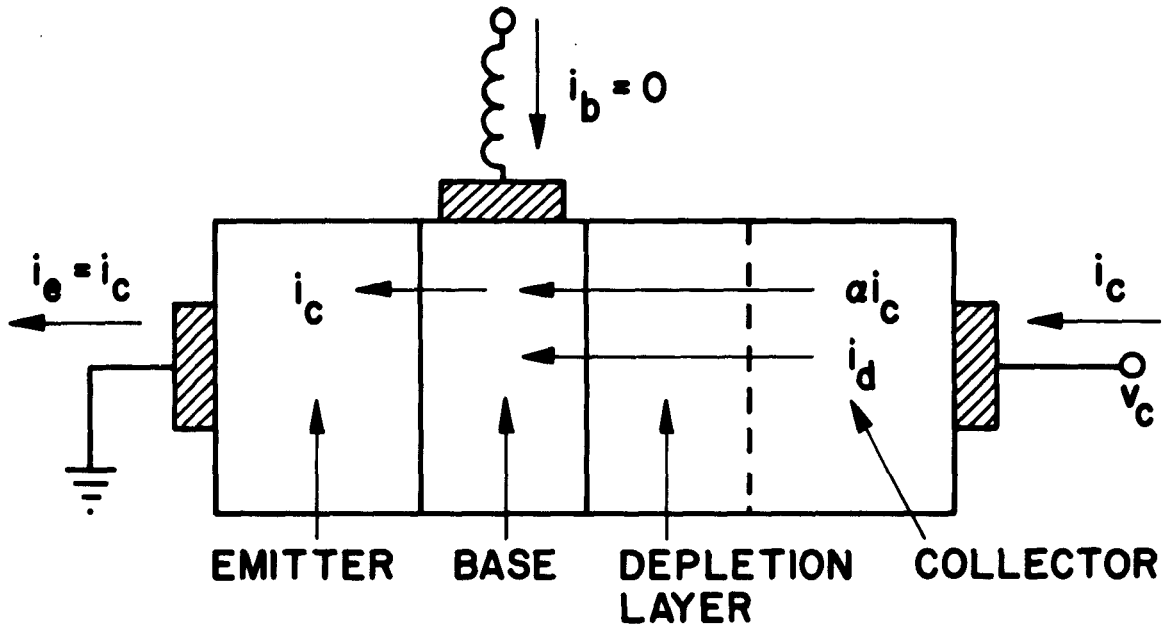

Fig. 1. Basic transit-time diode

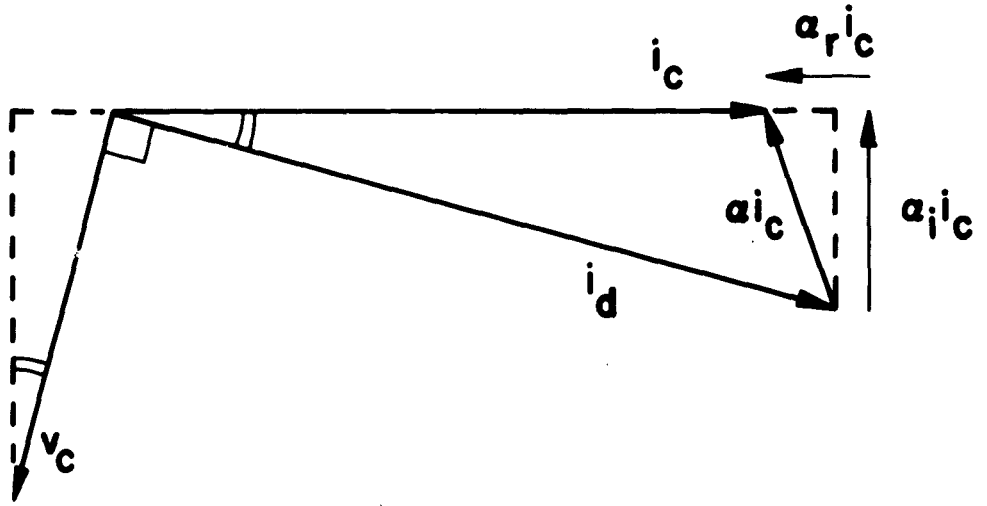

Fig. 2. Phasor diagram of currents

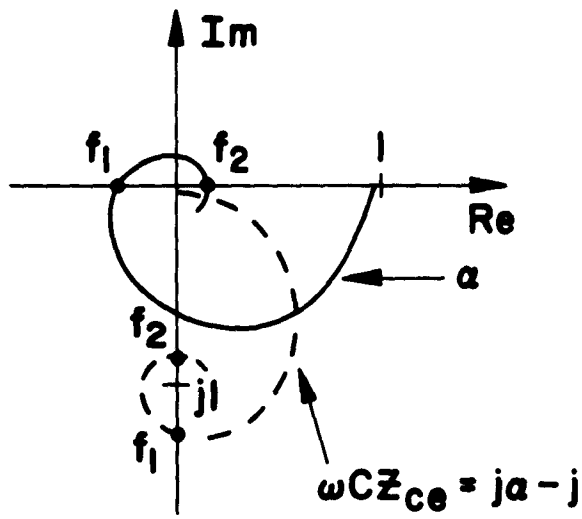

Fig. 3. Phasor plot of α and Z_{ce}

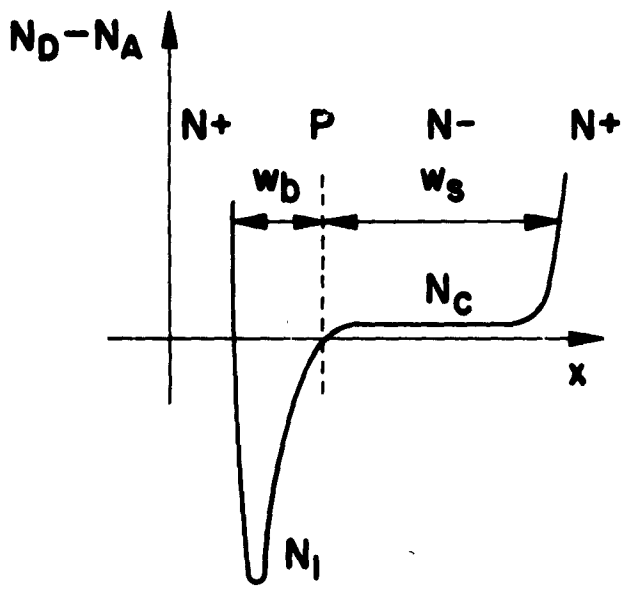

Fig. 4. Doping profile

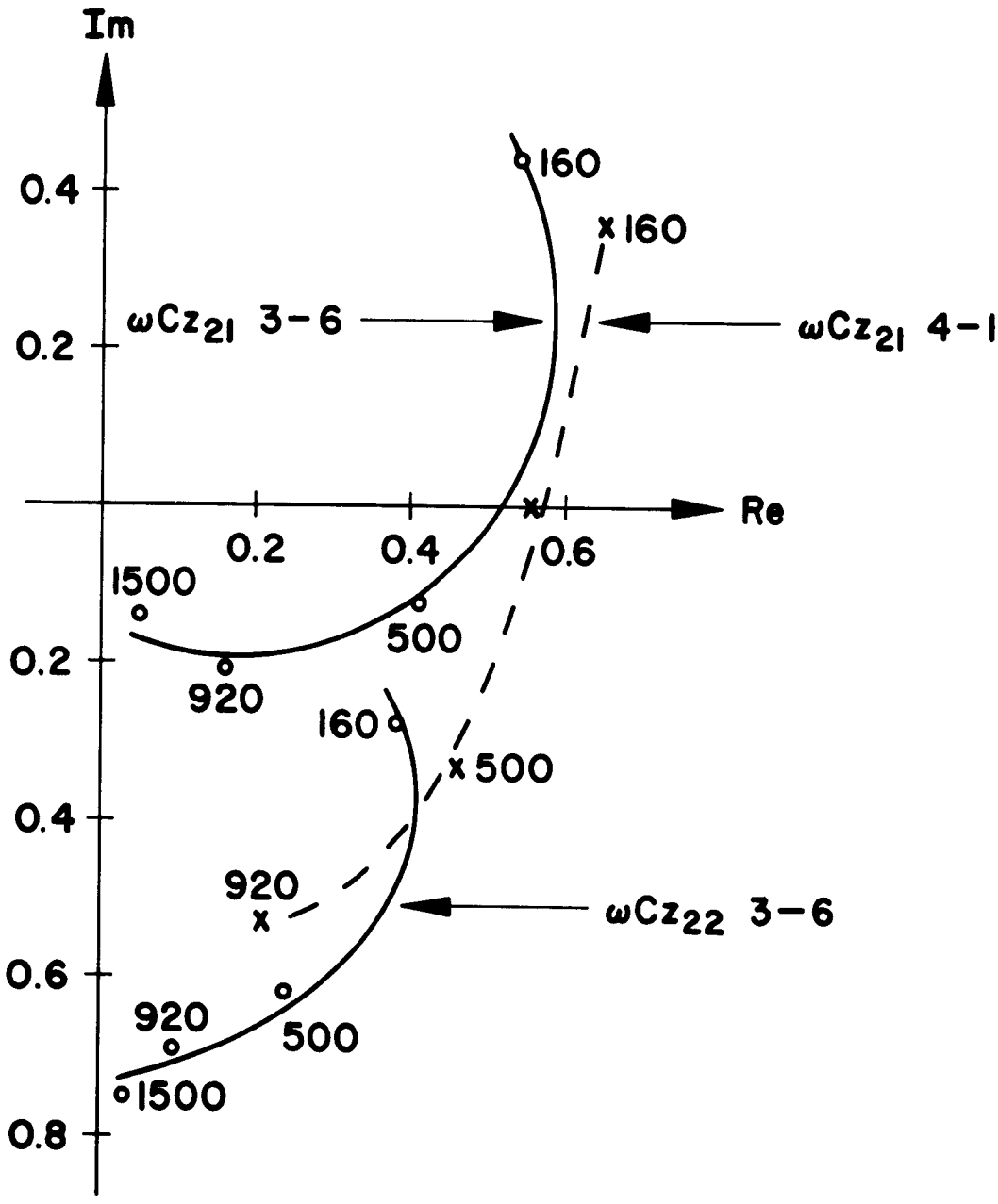

Fig. 5. Real and imaginary parts of ωCZ with frequency in Mc as a parameter

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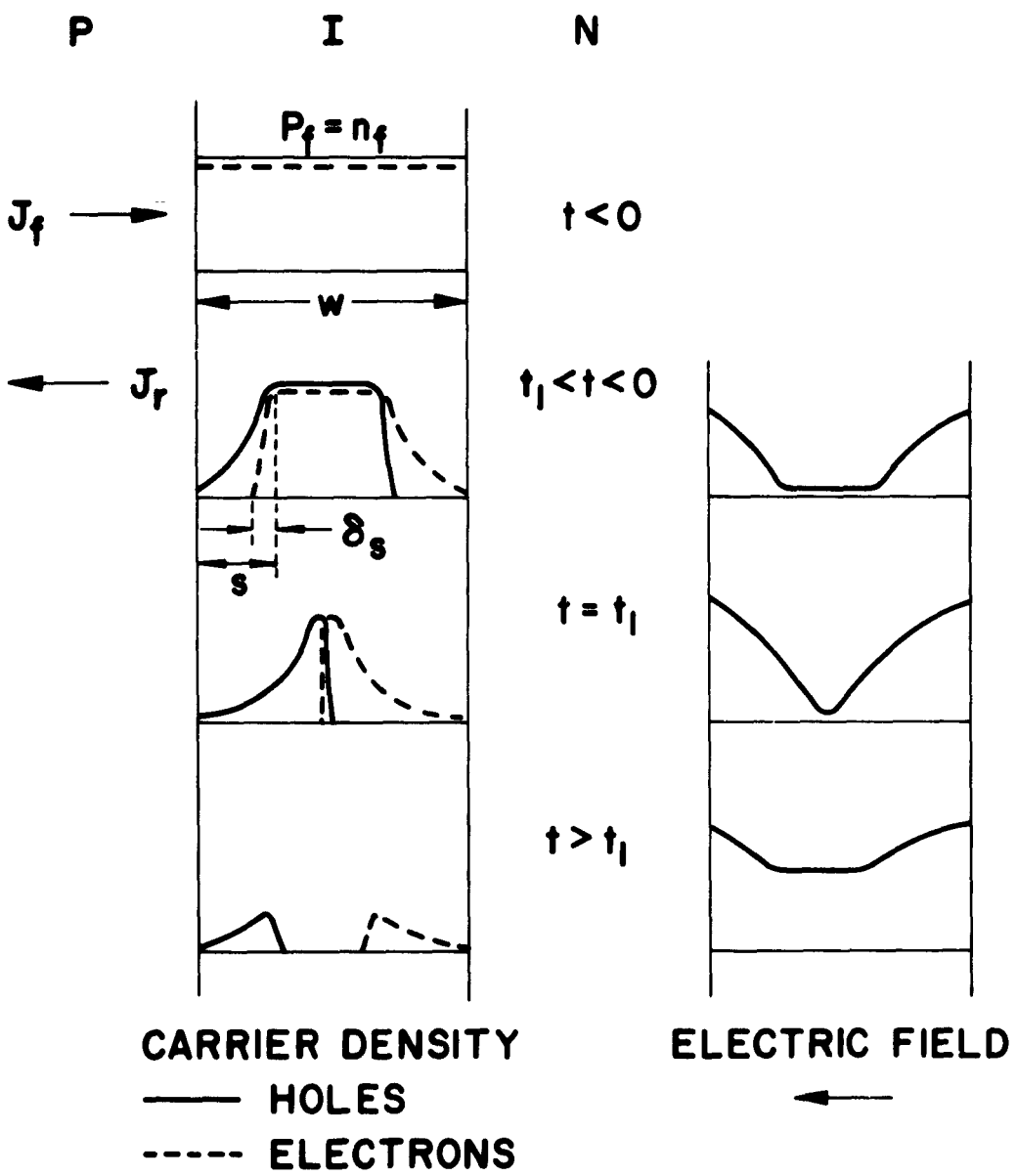

Fig. 6. Transient PIN carrier densities and electric field

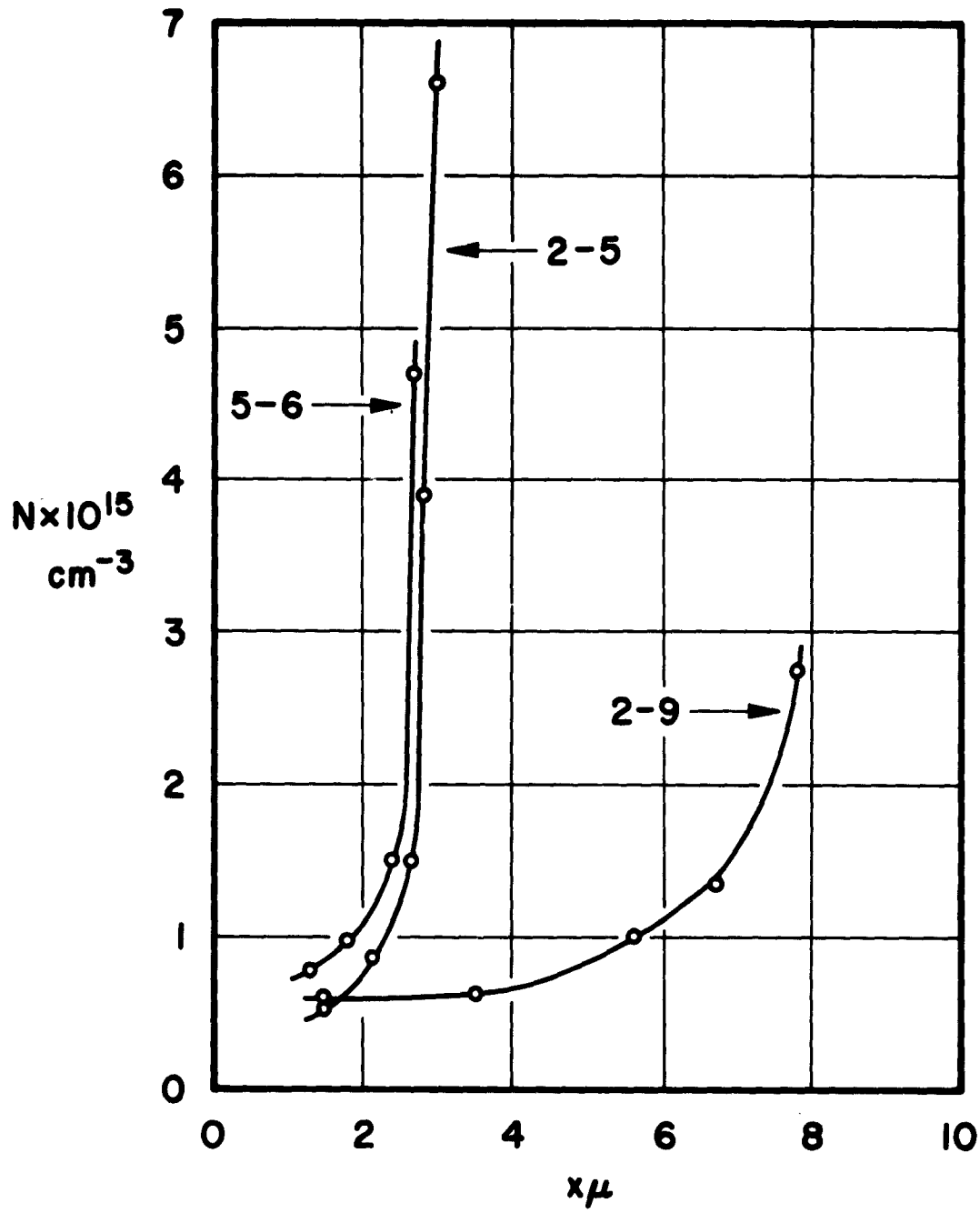

Fig. 7. N^- region doping density vs. distance

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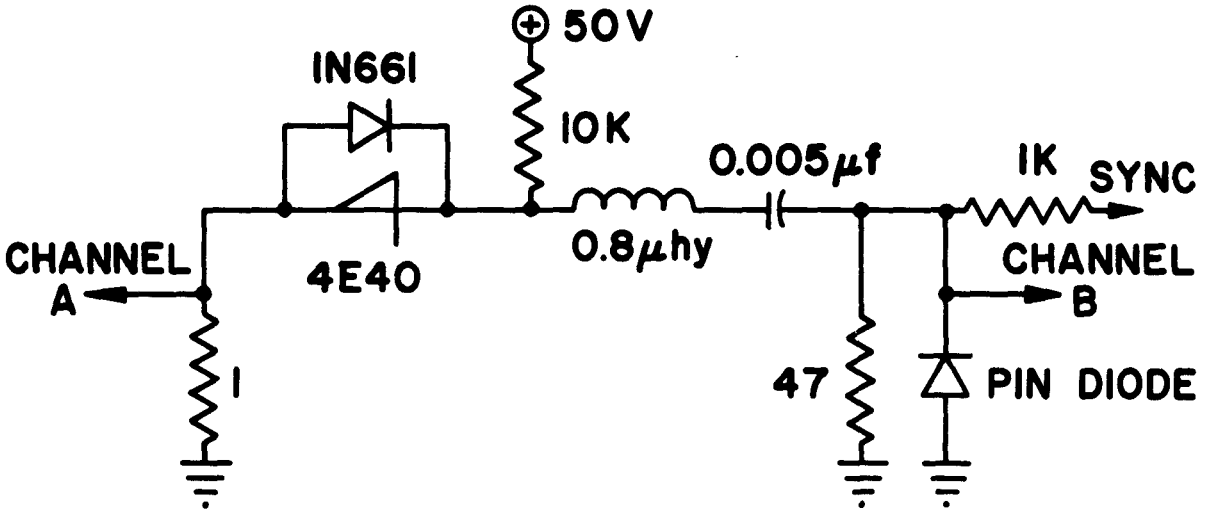


Fig. 8. PIN diode lifetime test circuit

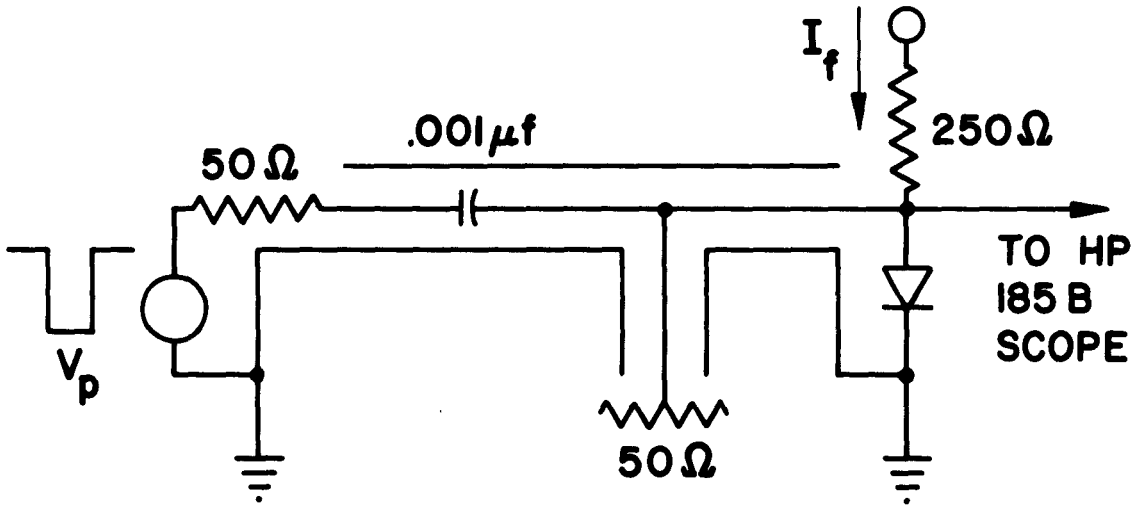
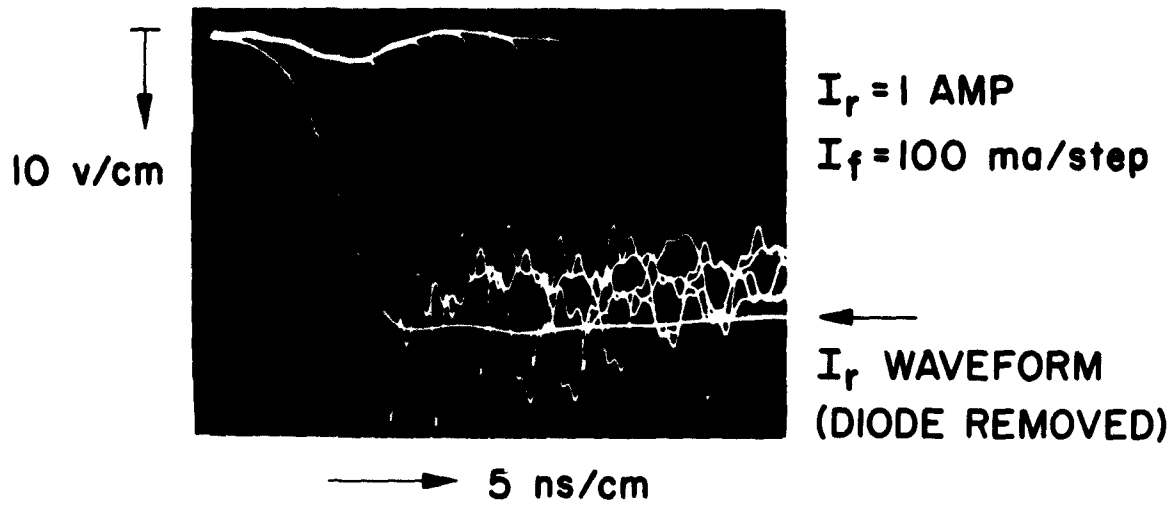


Fig. 9. PIN diode transition time test circuit.



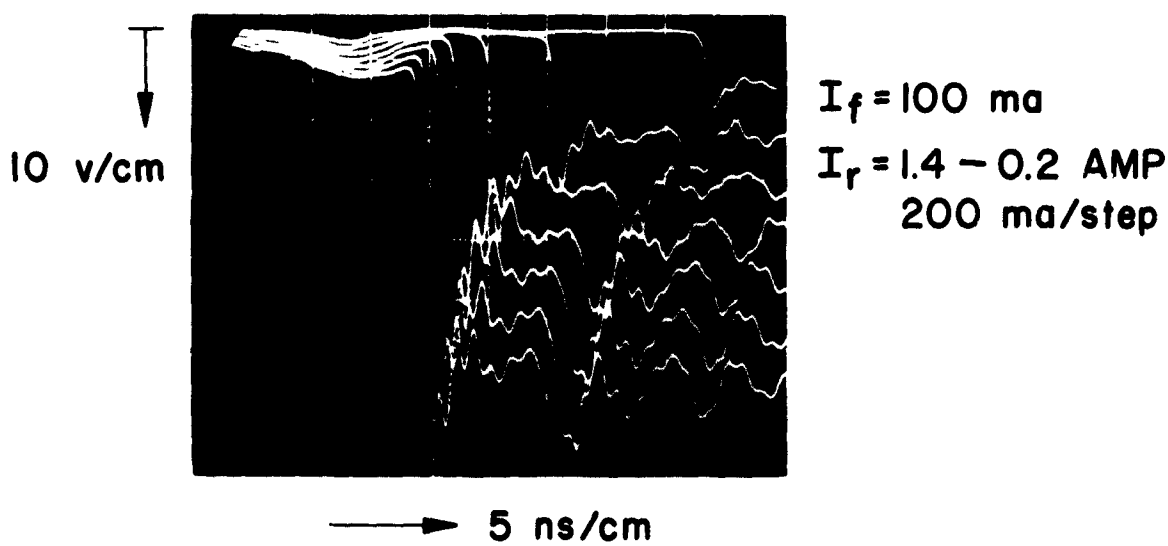


Fig. 10. Small-area diode storage and transition times

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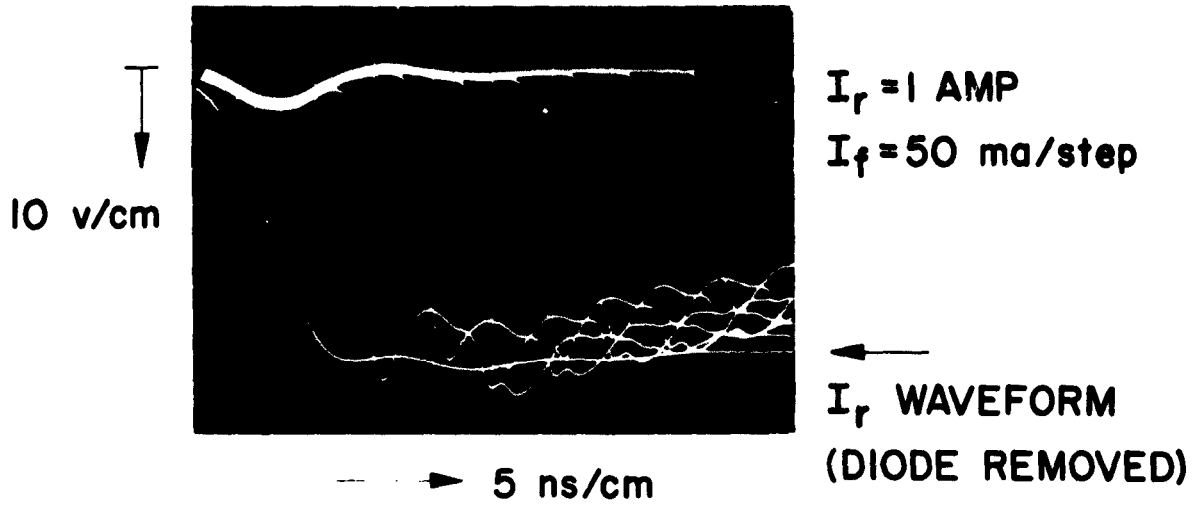

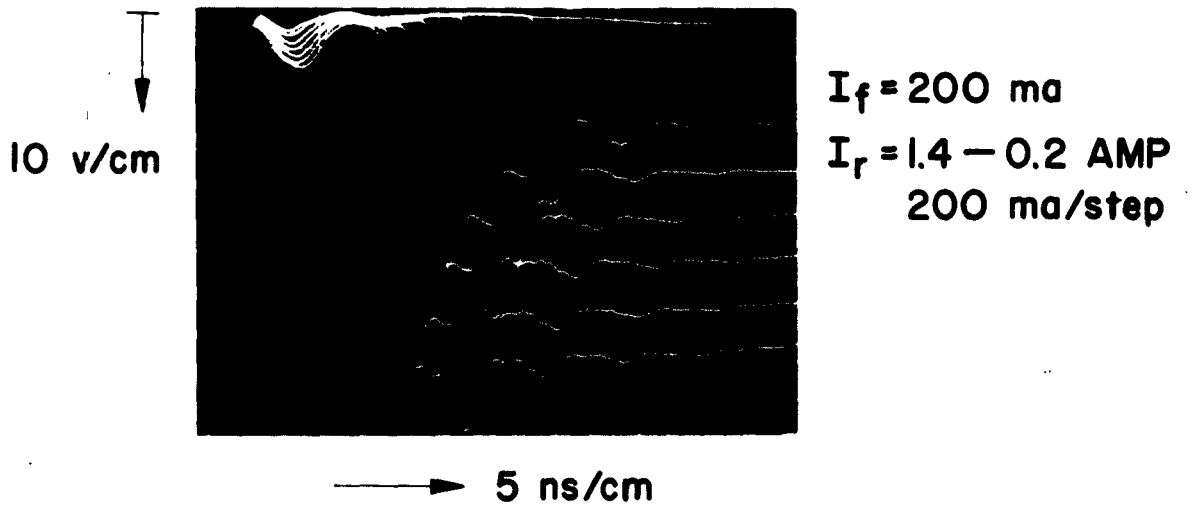

Fig. 11. Large-area diode storage and transition times

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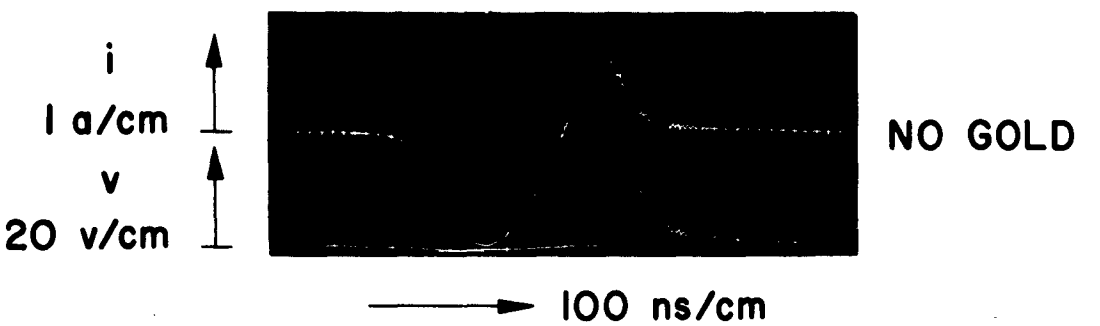

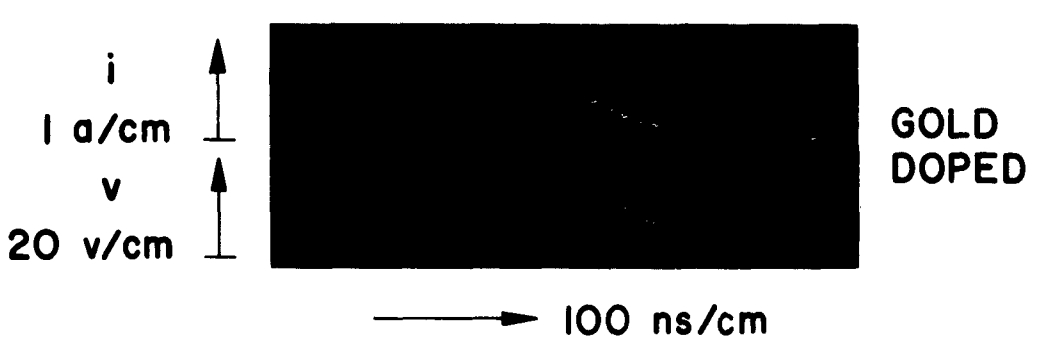

Fig. 12. Effect of gold doping on lifetime

AD_____

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NEW CONCEPTS FOR SOLID STATE MICROWAVE GENERATORS

First Quarterly Report, 1 October 1962 to 31 December 1962
Contract DA 36-039-AMC 00001(E) 33 pages incl. figs. Unclassified report

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The reverse recovery of a PIN diode is calculated and shown to be useful for harmonic generator applications. The transition time from on to off is determined by the transit time for carriers across the I region in space-charge limited flow, and by the diode capacitance. Experimental epitaxial diodes showed the expected performance of less than 1 ns turn-off time in a diode with 15 pf capacitance.

UNCLASSIFIED

1. Microwave oscillators
2. Diodes (semiconductors)
3. Transistors

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